# A 100 MHz to 500 MHz Low Noise Feedback Amplifier using ATF-54143

## Application Note 5057

**Introduction**

In the last few years the leading technology in the area of low noise amplifier design has been gallium arsenide (GaAs) devices, MESFET and pHEMT. Power amplifiers based on GaAs can achieve high efficiency and linearity, as well as providing high output power. Recently Enhancement Mode pHEMT technology has demonstrated industry leading power added efficiency (PAE) and linearity performance for amplifier applications. The E-pHEMT technology provides high gain and very low noise. The high gain at low frequencies enables the use of feedback to linearize the E-pHEMT device. This application note shows why E-pHEMT technology can provide superior electrical performance for low noise and high linearity amplifier design in UHF and VHF wireless communications bands.

**Design Goals**

The goal of the amplifier design is to produce a 100 to 500 MHz LNA with an output third order intercept point (OIP$_3$) of +36 dBm, a noise figure below 2.0 dB and 20 dB gain with a flat gain response. The use of RC feedback was used to provide good input and output match

and to ensure unconditional stability, with a second feature of offering a means of reducing the overall stage gain to the specified 20 dB level. The amplifier design specification includes operation from a 5V supply with current consumption of less than 65 mA.

The Avago ATF-54143 is one of a family of high dynamic range, low noise enhancement mode PHEMT discrete transistors designed for use in low cost commercial applications in the VHF through 6 GHz frequency range. It is housed in a 4-lead SC-70 (SOT-343) surface mount plastic package, and operates from a single regulated supply. If an active bias is desirable for repeatability of the bias setting—particularly desirable in high-volume production—the ATF-54143 requires only the addition of a single PNP bipolar junction transistor. Compared to amplifiers using depletion mode devices, the E-pHEMT design has a lower part count and a more compact layout. Besides having a very low typical noise figure (0.5 dB), the Avago ATF-54143 is specified at 2 GHz and 3-volt bias to provides a +36 dBm intercept point at 60 mA drain current. A data sheet for this device may be downloaded from: *http://literature.Avagotech.com/litweb/pdf/5989-0034EN.pdf*

**Low Noise E-pHEMT Amplifier Design**

Using Avago Technologies *EEsof Advanced Design System* software the amplifier circuit can be simulated in both linear and non-linear modes of operation. For the linear analysis the transistors can be modeled with a two-port s-parameter file using *Touchstone* format. More information about Avago EDA software may be found at: *http://www.Avagotech.com/eesof-eda*. The appropriate ATF54143.s2p file can be downloaded from the *Avago Wireless Design Center* web site: *http://www.semiconductor.Avagotech.com* (type ATF-54143 in the *Quick Search* at the top of the page. Under *Search Results* click on the underlined ATF-54143. Scroll down to the S-parameters listing for 60 mA).

For the non-linear analysis, a harmonic–balance (HB) simulation was used. HB is preferred over other non-linear methods because it is computationally fast, handles both distributed and lumped element circuitry, and can easily include higher-order harmonics and intermodulation products. HB was used for the simulation of the 1 dB compression point ($P_{-1dB}$) and output third order intercept point ($OIP_3$).

Although this non-linear transistor model closely predicts the DC and small signal behavior (including noise), it does not correctly predict the intercept point. To properly model the exceptionally high linearity of the E-pHEMT transistor, a better model is required.
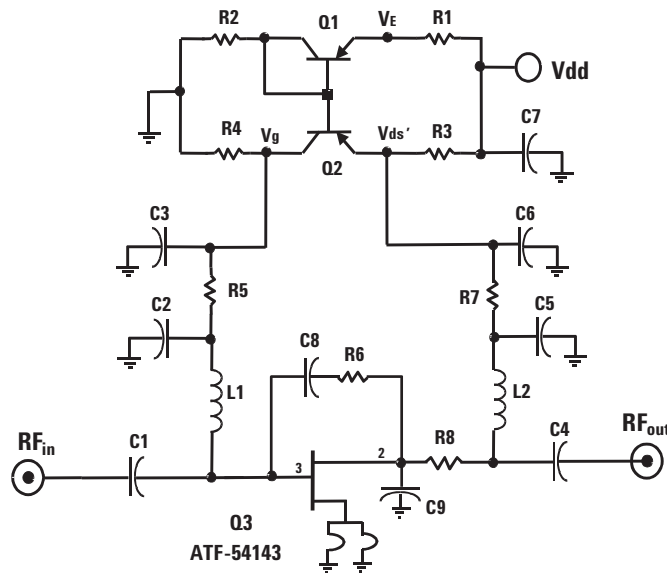


Figure 1.  ATF-54143 100-500 MHz HLA Active Bias Circuit Schematic.

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Besides providing information regarding gain, $P_{-1dB}$, noise figure, and input and output return loss, the simulation provides very important information regarding circuit stability. Unless a circuit is actually oscillating on the bench, it may be difficult to predict instabilities without actually presenting various VSWR loads at various phase angles to the amplifier. Calculating the Rollett stability factor (K) and generating stability circles are two methods made considerably easier with computer simulations. Simulated and measured results show the stability factor, K>1 (see Fig. 2), at the cost of reduced third-order intercept point and output power, through the use of a series resistor on the output.
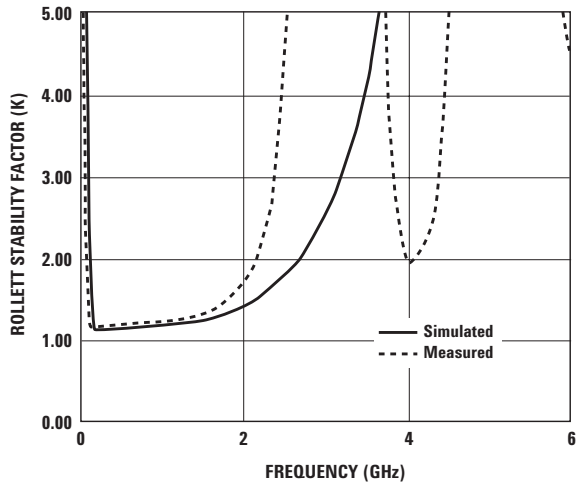
To meet the goals for noise figure, intercept point and gain, the drain source current ($I_{ds}$) was chosen to be 60 mA. The characterization data in the device data sheet shows that 60 mA gives the best $IP_3$ combined with a very low minimum noise figure ($F_{min}$). Also, as shown in the data sheet, a 3-V drain-to-source voltage ($V_{ds}$) gives a slightly higher gain and easily allows the use of a regulated 5-V supply.

The use of a controlled amount of source inductance, usually only a few tenths of a nanoHenry, can often be used to enhance LNA performance. This is effectively equivalent to increasing the source leads by approximately .025 inch or so. The effect can be easily modeled using an RF simulation tool such as ADS. The usual side effect of excessive source inductance is gain peaking at a high frequency and resultant oscillations.



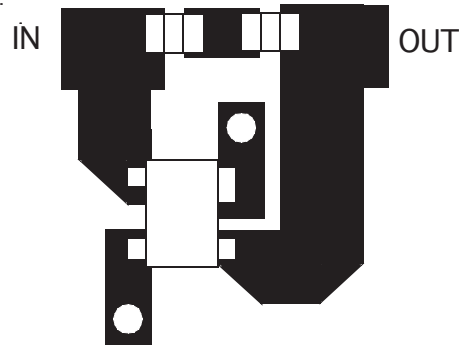Figure 2. Simulated and measured stability factor K.



Figure 3. Suggested RF layout to minimise inductance in feedback network.

### Active Bias

The main advantage of an active biasing scheme is the ability to hold the drain to source current constant over a wide range of temperature variations. A very inexpensive method of accomplishing this is to use two PNP bipolar transistors arranged in a current mirror configuration as shown in Fig. 1. Due to resistors R1 and R3 this circuit is not a *true* current mirror, but if the voltage drops across R1 and R3 are kept identical, the current through R3 is stabilized and therefore $I_{ds}$ and $V_{ds}$ are also kept stable. A passive bias network is discussed in Application Note 1222: *http://literature.Avagotech.com/litweb/pdf/5988-2336EN.pdf*

Transistor Q1 is configured with its base and collector tied together. This acts as a simple PN junction, which helps to temperature compensate the emitter-base junction of Q2. To calculate the values of R1, R2, R3, and R4 the following parameters must be known or chosen:

$I_{ds}$ is the device drain-to-source current, 60 mA.

$I_R$ is the reference current for active bias, 2.1 mA.

$V_{dd}$ is the power supply voltage, 5V.

$V_{ds}$ is the device drain-to-source voltage, 3.0V.

$V_{ds'}$ is used in the equations due to the voltage drop across R7 and R8, 3.56V.

$V_{gs}$ is the typical gate bias, 0.59V.

$V_{be1}$ is the typical base-emitter turn-on voltage for Q1 & Q2, 0.65V.

Therefore, resistor R3, which sets the desired device drain current, is calculated as follows:

$$(1) \quad R3 \approx \frac{V_{dd} - V_{ds'}}{I_{ds} + I_{c2}}$$

where $I_{C2}$ is chosen for stability to be 2.1 mA. This value is also equal to the reference current $I_R$.

The next three equations are used to calculate the rest of the biasing resistors for Fig. 1.

$$(2) \quad R1 \approx \frac{V_{dd} - V_{ds'}}{I_R}$$

Note that the voltage drop across R1 must be set equal to voltage drop across R3, but with a current of $I_R$.

$$(3) \quad R2 \approx \frac{V_{ds'} - V_{be1}}{I_R}$$

R2 sets the bias current through Q1.

$$(4) \quad R4 \approx \frac{Vg}{I_{c2}}$$

R4 sets the gate voltage. $I_{c2} = I_{e2}$ assuming the $h_{fe}$ of the PNP -transistors is high. Calculated resistor values differ from actual resistors due to available component values.

**Table 1.  Component Parts List.**

| | |
|---|---|
| C1=150 pF | 0603 Chip Capacitor |
| C2, C5=68 pF | 0603 Chip Capacitor |
| C3, C6=10 nF | 0603 Chip Capacitor |
| C4=100 pF | 0603 Chip Capacitor |
| C7=1 µF | 0603 Chip Capacitor |
| C8=180 pF | 0402 Chip Capacitor |
| C9=2.2 pF | 0402 Chip Capacitor |
| L1=150 nH | TOKO LL1608-FSR15 |
| L2=120 nH | TOKO LL1608-FSR12 |
| R1=680Ω | 0603 Chip Resistor |
| R2=1300Ω | 0603 Chip Resistor |
| R3=22Ω | 0603 Chip Resistor |
| R4=270Ω | 0603 Chip Resistor |
| R5=47Ω | 0603 Chip Resistor |
| R6=680Ω | 0402 Chip Resistor |
| R7, R8=4.7Ω | 0603 Chip Resistor |
| Q1, Q2 | Phillips Semiconductor BCV62C |
| Q3 | Avago ATF-54143 |

Input and output RF connectors are EF Johnson end-launch SMA connectors (p.n. 142-0701-881).

The numbers associated with the chip capacitors and resistors refer to the dimensions of the components: 0402 = 40 x 20 mil, etc.

Thus by forcing the emitter voltage ($V_E$) of transistor Q1 equal to $V_{ds}$, this circuit regulates the drain current in a manner similar to a current mirror. As long as Q2 operates in the forward active mode, this hold true. In other words the collector-base junction of Q2 must be kept reversed biased.

An evaluation board was designed for the feedback amplifier network. This single-layer board (see Figs. 4 and 5) is 0.031-inch thickness FR-4 material with a dielectric constant of 4.2. The feedback network should be made as short as possible, since introducing inductance into the feedback network will cause instability in the 5-6 GHz region. The RC feedback uses 40 x 20 mil components that are soldered close together with a small solder pad in between.

The ATF-54143 is *conditionally* stable below 3.5 GHz, having 29-26 dB gain in the 100-500 MHz region. The R-C feedback reduces low frequency gain and increases the stability factor to >1 below 2 GHz. The amplifier uses a high-pass impedance matching network, consisting of C1 and L1, for the noise match. The circuit loss will directly relate to noise figure, thus the Q of L1 is extremely important. The Toko LL1608-FSR15 is a small multi-layer chip inductor with a rated Q of 19 at 50 MHz. The shunt inductor (L1) provides low frequency gain reduction, which can minimize the amplifier's susceptibility to overload from nearby low frequency transmitters; it is also part of the input matching network along with C1. C1 also doubles as a DC block, while L1 also provides a means of inserting gate voltage for the PHEMT. This requires a good bypass capacitor in the form of C2.
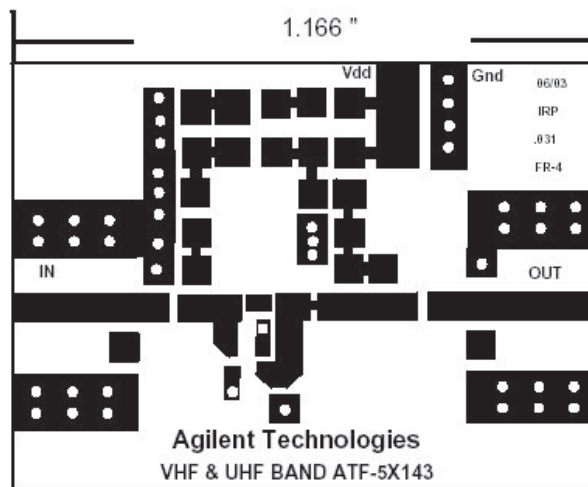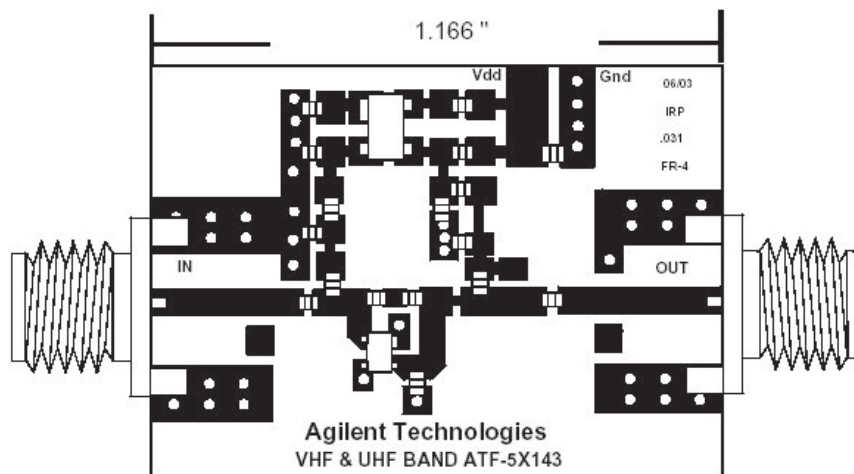


Figure 4.  RF Layout for Demo Board.



Figure 5.  Assembly Drawing for Amplifier.

This network represents a compromise between noise figure, input return loss and gain. Capacitors C2 and C5 provide in-band stability while resistors R5 and R7 provide low-frequency stability by providing a resistive termination. The high-pass network on the output consists of a series capacitor C4 and shunt inductors L2, with L2 also providing a means of inserting drain voltage for biasing up the PHEMT. Very short transmission lines between each source lead and ground have been used. The RC-feedback has a dramatic effect on in-band and out-of-band gain, stability and input and output return loss.

**Simulated vs. Actual Performance of the E-pHEMT Broadband LNA**

Results from the simulation of gain, NF and for input and output return loss are shown in Figs. 6 and 7, respectively. Measured gain and noise figure and input and output return loss appear in Figs. 8 and 9, respectively. A summary of the measured results is shown in Table 2.
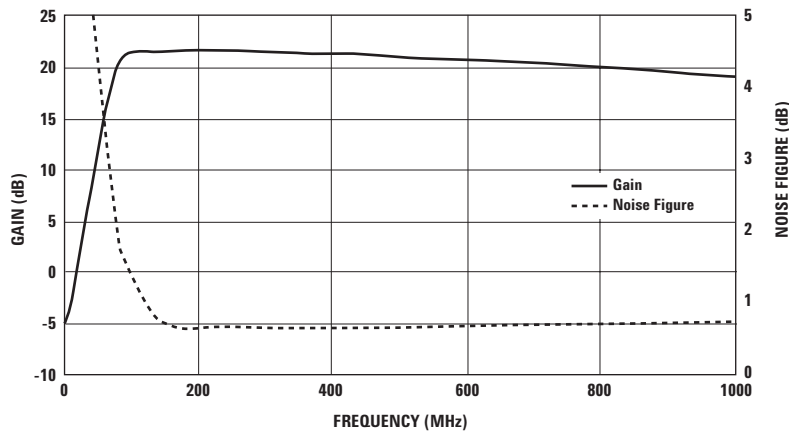
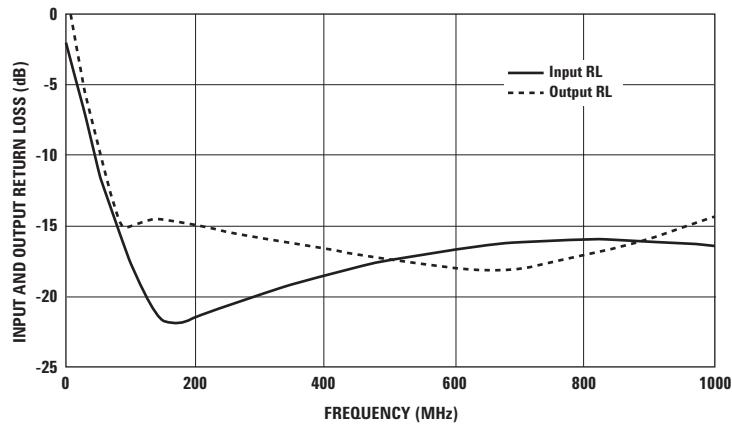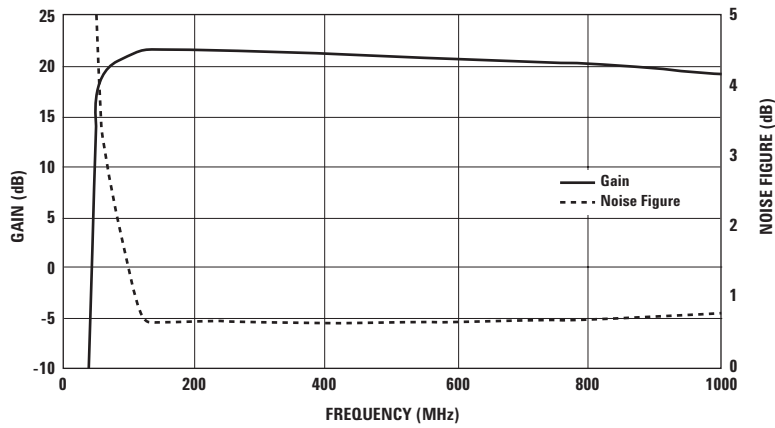

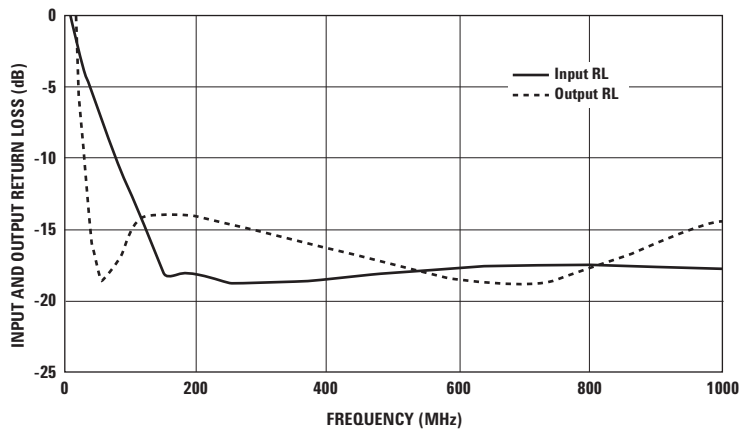Figure 6. Simulation Results for Gain and Noise Figure.



Figure 7. Simulation Results for Input and Output Return Loss.

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**Table 2. Measured Results.**

| Frequency (MHz) | Gain (dB) | NF (dB) | P1dB (dBm) | OIP3 (dBm) |
|---|---|---|---|---|
| 100 | 20.8 | 1.20 | +16.6 | +34.5 |
| 200 | 21.1 | 0.67 | +16.6 | +36.3 |
| 300 | 21.4 | 0.62 | +16.6 | +36.5 |
| 400 | 21.2 | 0.61 | +16.6 | +36.1 |
| 500 | 20.5 | 0.70 | +16.8 | +36.5 |



**Figure 8. Measured Results for Gain and Noise Figure.**



**Figure 9. Measured Results for Input and Output Return Loss.**

**References**

[1] Applications Note AN-1222: A Low Noise High Intercept Point Amplifier for 1930 to 1990 MHz using the ATF-54143 PHEMT— A.J. Ward

[2] Stephan Maas, Nonlinear Microwave circuits, IEEE Press, New York 1997

[3] W. R. Curtice, "A MESFET model for use in the design of GaAs integrated circuits," *IEEE Trans Microwave Theory Tech*, vol. MTT-28, pp. 448-456, May 1980.

Avago Eesof Advanced Design System (ADS) electronic design automation (EDA) software for system, RF, and DSP designers who develop communications products. More information about Avago EDA software may be found on *http://www.Avagotech.com/eesof-eda.*

Performance data for Avago ATF-54143 may be found on *http://www.Avagotech.com/view/rf*

For product information and a complete list of distributors, please go to our web site:
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